

# Unit - 03

## Control Unit

Instruction set:- The operation of the processor is determined by the instruction that it executes known as machine instruction or computer instruction.

- The collection of different instructions that processor can execute is referred to as a processor instruction set.
- A computer instruction is a binary code that instructs the computer to perform a specific operation.

### Types of instructions:-

The computer instruction can be classified into three categories -

- 1) Data Transfer Instruction
- 2) Data Manipulation Instruction
- 3) Program Control Instruction

Data Transfer Instruction:- possess transfer of data from one location to another without changing the binary information content.

Data manipulation instructions are those that perform arithmetic, logic and shift operation.

Program Control instructions provide decision making capabilities and change the path taken by the program when executed.

### DATA TRANSFER INSTRUCTION

Data transfer instruction move the data from one location to another without changing the source content.

- These instructions are used to bring the data to and from memory to register.

Example:-

- ① MOVE:- It denotes transfer of data from one register to another
- ② STORE:- Transfer from a processor register into memory
- ③ LOAD:- A transfer from memory to register.
- ④ Exchange:- It swaps information between the two registers or a register and memory.

- ⑤ Input:- Transfer from input terminal to processor register.
- ⑥ Output:- Transfer from processor register to output terminal.
- ⑦ PUSH:- Transfer from processor register to top of the stack.
- ⑧ POP:- Transfer from top of the stack to the processor register.
- ⑨ clear:- Transfer of word zeros to the destination.
- ⑩ SET:- Transfer of words once to the destination.

- ①  $\text{MOV } R_1, [\text{MEM}] \Rightarrow$  Memory to register transfer
- ②  $\text{MOV}[\text{MEM}], R_2 \Rightarrow$  Register to memory transfer
- ③  $\text{MOV } R_1, R_2 \Rightarrow$  Register to register transfer
- ④  $\text{IN } R, \text{PORT} \Rightarrow$  Read from an I/O PORT
- ⑤  $\text{OUT PORT}, R_2 \Rightarrow$  Write from an I/O PORT

Data Manipulation Instruction :-

Data manipulation instructions perform operation on the data.

These can be divided into three types-

i) Arithmetic operation or instruction.

ii) Logical and bit manipulation instruction

iii) Shift operation

1) Arithmetic instruction:- These instructions are used to perform arithmetic operation.

For EX:-

- a) Add:- It perform the addition of two operands.
- b) Subtract:- It perform difference of two operand.
- c) Multiply:- It performs product of two operands.
- d) Division:- It performs the division of two operands and calculate quotient and remainder.
- e) Add with carry:- It compute the sum of two operands with carry.
- f) Subtract with borrow:- It compute the difference with borrow.
- g) Increment:- Add 1 to the operand.
- h) Decrement:- subtract 1 from operand.
- i) ~~2~~ Negate (2's complement):- It changes the sign of the operand.

EX-  
ADD R1, R2  
SUB R1, R2  
MUL R1, R2  
INC R1  
DEC R1

2) Logical instructions:-

- These perform logical and bit manipulation instruction on the bits of the data.
- They perform binary operations on the string of bits stored in the register.

For EX:- AND, OR, NAND, NOR, NOT, EX-OR, EX-NOR

EX:- AND R1, R2 → It performs AND operation bitwise on R1, R2.

3) Shift micro operation:-

The operation in which the bits of the word are moved to the left or right.

EX:- Logical shift left; Logical shift right,  
Arithmetic shift left; Rotate left,  
Arithmetic shift right; rotate right

## Program Control Instruction

• A program control is a type of instruction when executed may change the address value in the program counter and causes the flow of control to be altered.

• These instructions specify conditions for altering the content of the program counter.

Ex. a) Jump (Branch):- Unconditional transfer, load PC with the specified address

b) Jump (conditional):- Test specified conditions, either load PC with specified address or do nothing based on the conditions.

c) Return:- Replace content of the PC and other registers from the known locations.

d) Skip:- Increment to PC to skip the next instruction.

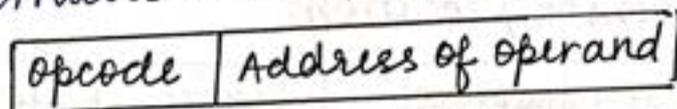
e) skip (conditional):- Test specified conditions either skip or do nothing based on the condition.

f) Halt:- Stop program execution.

g) No operation:- No operation is performed but program execution is continue.

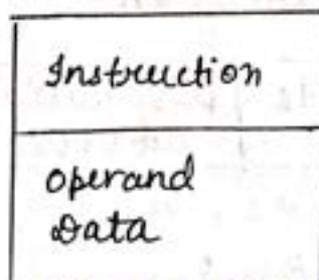
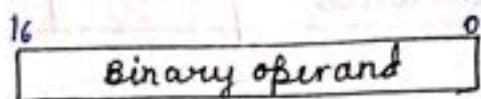
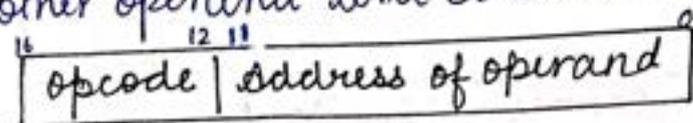
## Stored Program Organization OR Processor Organization with accumulator OR Single Accumulator Organization

To organize a computer in this method processor has a register called accumulator and an instruction code format with two parts



The first part specify the operation to be performed and the second one specify an address of operand in memory.

The other operand will be store in the processor register.



Memory =  $4096 \times 16$

$= 2^{12} \times 16$   
↓  
Address bit

In this method the processor performs the operation specified by the opcode on the data specified/stored on the memory location and the content of the accumulator register.

### Instruction format :-

The most common fields on the instruction are

Opcode	Address of operand	Mode
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- operation field (opcode) specify the operation to be performed.
- Address field which contains the location of the operand (register or memory location).
- Mode Field which specifies how operand is to be found.

Note:- Generally CPU organizations are -

- 1) General register organization
  - 2) Stack organization
  - 3) Single Accumulator Organization
- An instruction is of various length depending upon the number of addresses it contains.
  - On the basis of no. of addresses instruction can be classified as:-
    - 1) 3- Address instructions
    - 2) 2- Address instructions
    - 3) 1- Address instruction
    - 4) Zero Address instruction

1) 3- Address Instruction:- This format of the instruction has three addresses to specify a register or memory location.

opcode	Destination Address	Source Address	Source Address	Mode
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Ex- ADD R<sub>1</sub>, R<sub>2</sub>, R<sub>3</sub>

2) 2-Address Instruction:-

opcode	Destination Address	Source Address	Mode
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Ex:-  
MOV R<sub>1</sub>, A  
ADD R<sub>1</sub>, B

### 3) 1-Address Instruction :-

Opcode	Address of operand	Mode
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- It has only one address to specify a register or a memory location
- This uses an accumulator register to store one operand or intermediate result.

Ex:- Load A  
ADD B

### 4) Two Address Instruction :-

- This format does not contain any address field.
- The stack based computers do not use address field in the instruction to perform operation because the operation is performed on the two top items of the stack.

Ex:- 

Opcode
--------

• ADD

Q) Write the program by using -

- 3-Address Instruction
- 2-Address Instruction
- 1-Address Instruction
- 0-Address Instruction

$$X = (A+B) * (C+D)$$

Ans) 3 Address Instruction

```
ADD R1, A, B
ADD R2, C, D
MUL X, R1, R2
```

```
R1 ← M[A] + M[B]
R2 ← M[C] + M[D]
X ← R1 * R2
```

2 Address Instruction

```
MOV R1, A
ADD R1, B
MOV R2, C
ADD R2, D
MUL R1, R2
MUL X, R1
```

```
R1 ← M[A]
R1 ← R1 + M[B]
R2 ← M[C]
R1 ← R2 * R2
M[X] ← R1
```

### 3) One Address Instruction.

LOAD A	$AC \leftarrow M[A]$
ADD B	$AC \leftarrow AC + M[B]$
<del>LD</del> STORE T	$M[T] \leftarrow AC$
LOAD C	$AC \leftarrow M[C]$
ADD D	$AC \leftarrow AC + M[D]$
MUL T	$AC \leftarrow AC * M[T]$
STORE X	$M[X] \leftarrow AC$

### 4) Zero Address Instruction

$$X = (A+B) * (C+D)$$

Prefix Exp  $\Rightarrow X = A B + C D + *$

PUSH A	Top = A
PUSH B	Top = B
ADD	Top = A+B
PUSH C	Top = C
PUSH D	Top = D
ADD	Top = C+D
MUL	Top = (A+B)*(C+D)
POP X	M[X] = Top

Q2]  $X = (A-B) + C * (D * E - F) / (G+H * K)$

$$\frac{(A-B) + C * (D * E - F)}{G+H * K}$$

OR

### Ans) 3 Address Instruction:-

SUB R <sub>1</sub> , A, B
MUL R <sub>2</sub> , D, E
SUB R <sub>2</sub> , R <sub>2</sub> , F
MUL R <sub>2</sub> , R <sub>2</sub> , C
ADD R <sub>2</sub> , R <sub>1</sub> , R <sub>2</sub>
MUL R <sub>3</sub> , H, K
ADD R <sub>3</sub> , R <sub>3</sub> , G
DIV X, R <sub>3</sub> , R <sub>2</sub>

### 2 Address Instruction

MOV R <sub>1</sub> , A	
SUB R <sub>1</sub> , B	
MOV R <sub>2</sub> , D	
MUL R <sub>2</sub> , E	
SUB R <sub>2</sub> , F	
MUL R <sub>2</sub> , C	
ADD R <sub>1</sub> , R <sub>2</sub>	
MOV R <sub>3</sub> , H	<del>STORE X</del>
MUL R <sub>3</sub> , K	
ADD R <sub>3</sub> , G	
DIV R <sub>1</sub> , R <sub>3</sub>	STORE X, R <sub>3</sub>

1 Address

LOAD A  
 SUB B  
 STORE T  
 LOAD D  
 MUL E  
 SUB F  
 MUL C  
 STORE T  
 ADD T  
 LOAD H  
 MUL K  
 ADD G  
 STORE T<sub>1</sub>  
 LOAD T  
 DIV T  
 STORE X

Zero Address

$AB - CDE * F - * + G HK * + /$   
 PUSH A  
 PUSH B  
 SUB  
 PUSH C  
 PUSH D  
 PUSH E  
 MUL  
 PUSH F  
 SUB  
 MUL  
 ADD  
 PUSH G  
 PUSH H  
 PUSH K  
 MUL  
 ADD  
 DIV  
 POP

$$2) X = A * B + C * D + E * F$$

3 Address

MUL R<sub>1</sub>, A, B  
 MUL R<sub>2</sub>, C, D  
 MUL R<sub>3</sub>, E, F  
 ADD R<sub>2</sub>, R<sub>2</sub>, R<sub>3</sub>  
 ADD X, R<sub>1</sub>, R<sub>2</sub>

2 Address

MOV R<sub>1</sub>, A  
 MUL R<sub>1</sub>, B  
 MOV R<sub>2</sub>, C  
 MUL R<sub>2</sub>, D  
 MOV R<sub>3</sub>, E  
 MUL R<sub>3</sub>, F  
 ADD R<sub>2</sub>, R<sub>3</sub>  
 ADD R<sub>1</sub>, R<sub>2</sub>  
 MOV X, R<sub>1</sub>

1 Address

LOAD A  
 MUL B  
 STORE T  
 LOAD C  
~~LOAD~~ MUL D  
 STORE T<sub>1</sub>  
 LOAD E  
 LOAD F  
 STORE T<sub>2</sub>  
 LOAD T  
 ADD T<sub>1</sub>  
 ADD T<sub>2</sub>  
 STORE X

Postfix

$AB * CD * + EF * +$

PUSH A  
 PUSH B  
 MUL  
 PUSH C  
 PUSH D  
 MUL  
 ADD  
 PUSH E  
 PUSH F  
 MUL  
 ADD  
 POP